2N7002

60 V, 300 mA N-channel Trench MOSFET

Rev. 7 — 8 September 2011 **Product data sheet**

1. Product profile

1.1 General description

N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using Trench MOSFET technology.

1.2 Features and benefits

- Suitable for logic level gate drive sources
- Very fast switching
- Surface-mounted package
- Trench MOSFET technology

1.3 Applications

- Logic level translators
- High-speed line drivers

1.4 Quick reference data

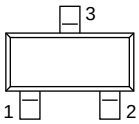
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C	-	-	60	V
I_D	drain current	V_{GS} = 10 V; T_{sp} = 25 °C; see Figure 1; see Figure 3	-	-	300	mA
P_{tot}	total power dissipation	T_{sp} = 25 °C; see Figure 2	-	-	0.83	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 500 mA; T_j = 25 °C; see Figure 6; see Figure 8	-	2.8	5	Ω

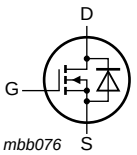
2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	S	source		
3	D	drain		



SOT23 (TO-236AB)



3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
2N7002	TO-236AB	plastic surface-mounted package; 3 leads	SOT23

4. Marking

Table 4. Marking codes

Type number	Marking code[1]
2N7002	12%

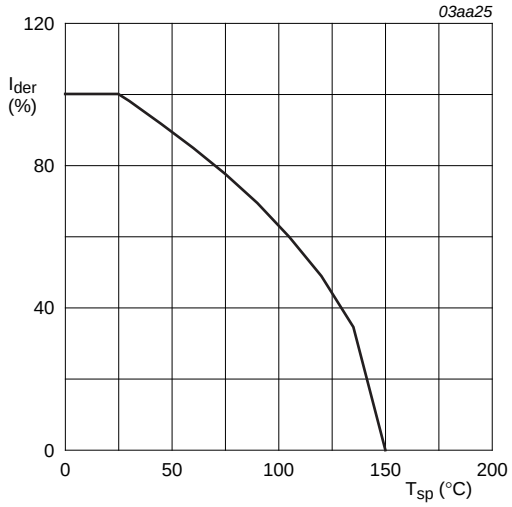
[1] % = placeholder for manufacturing site code

5. Limiting values

Table 5. Limiting values

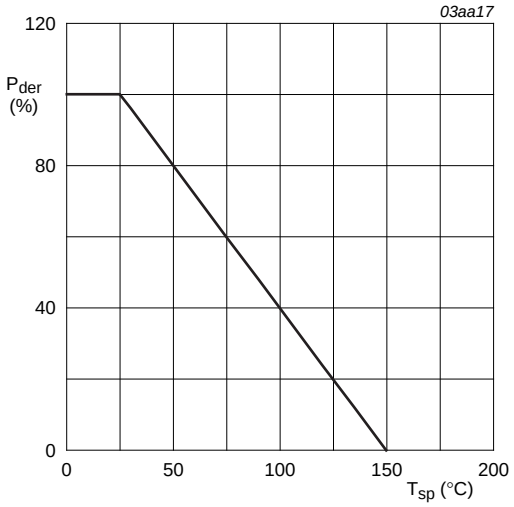
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C	-	60	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ	-	60	V
V_{GS}	gate-source voltage		-30	30	V
V_{GSM}	peak gate-source voltage	pulsed; t_p ≤ 50 µs; δ = 0.25	-40	40	V
I_D	drain current	V_{GS} = 10 V; T_{sp} = 25 °C; see Figure 1; see Figure 3	-	300	mA
		V_{GS} = 10 V; T_{sp} = 100 °C; see Figure 1	-	190	mA
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{sp} = 25 °C; see Figure 3	-	1.2	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; see Figure 2	-	0.83	W
T_j	junction temperature		-65	150	°C
T_{stg}	storage temperature		-65	150	°C
Source-drain diode					
I_S	source current	T_{sp} = 25 °C	-	300	mA
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{sp} = 25 °C	-	1.2	A



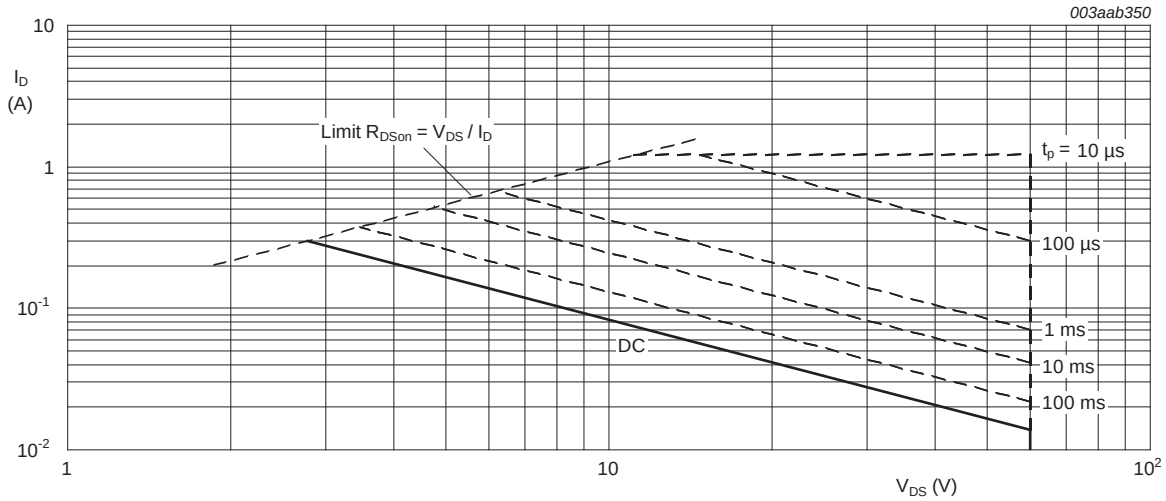
$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

Fig 1. Normalized continuous drain current as a function of solder point temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature



$T_{sp} = 25\,°C; I_{DM}$ is single pulse

Fig 3. Safe operating area; continous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	Mounted on a printed-circuit board; minimum footprint ; vertical in still air	-	-	350	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 4	-	-	150	K/W

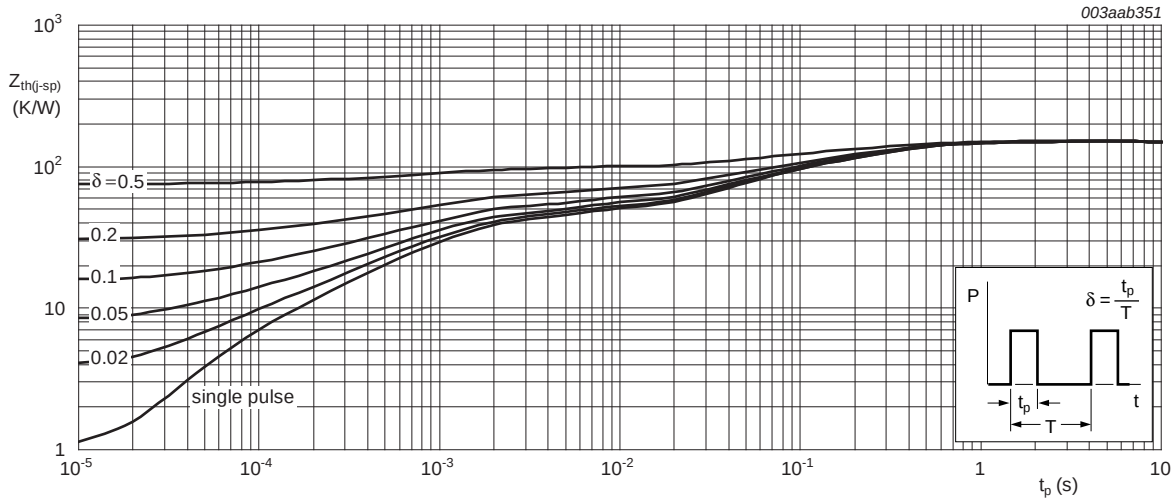
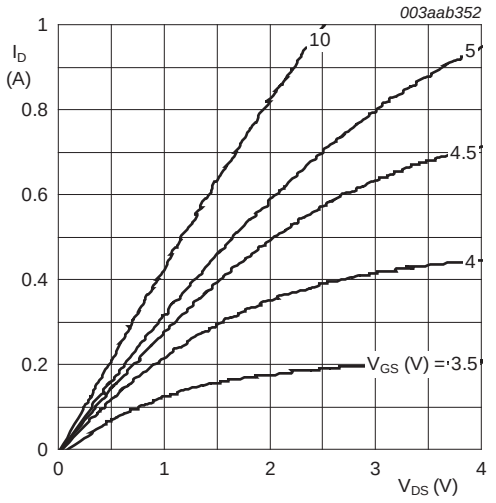


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

7. Characteristics

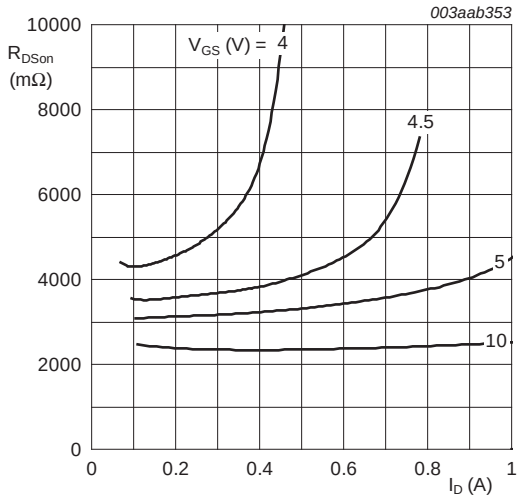
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 µA; V_{GS} = 0 V; T_j = 25 °C	60	-	-	V
		I_D = 10 µA; V_{GS} = 0 V; T_j = -55 °C	55	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = 0.25 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 9; see Figure 10	1	2	2.5	V
		I_D = 0.25 mA; V_{DS} = V_{GS}; T_j = 150 °C; see Figure 9; see Figure 10	0.6	-	-	V
		I_D = 0.25 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 9; see Figure 10	-	-	2.75	V
I_{DSS}	drain leakage current	V_{DS} = 48 V; V_{GS} = 0 V; T_j = 25 °C	-	0.01	1	µA
		V_{DS} = 48 V; V_{GS} = 0 V; T_j = 150 °C	-	-	10	µA
I_{GSS}	gate leakage current	V_{GS} = 15 V; V_{DS} = 0 V; T_j = 25 °C	-	10	100	nA
		V_{GS} = -15 V; V_{DS} = 0 V; T_j = 25 °C	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 500 mA; T_j = 25 °C; see Figure 6; see Figure 8	-	2.8	5	Ω
		V_{GS} = 10 V; I_D = 500 mA; T_j = 150 °C; see Figure 6; see Figure 8	-	-	9.25	Ω
		V_{GS} = 4.5 V; I_D = 75 mA; T_j = 25 °C; see Figure 6; see Figure 8	-	3.8	5.3	Ω
Dynamic characteristics						
C_{iss}	input capacitance	V_{DS} = 10 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C	-	31	50	pF
C_{oss}	output capacitance		-	6.8	30	pF
C_{rss}	reverse transfer capacitance		-	3.5	10	pF
t_{on}	turn-on time	V_{GS} = 10 V; V_{DS} = 50 V; R_L = 250 Ω; $R_{G(ext)}$ = 50 Ω; R_{GS} = 50 Ω	-	2.5	10	ns
t_{off}	turn-off time		-	11	15	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 300 mA; V_{GS} = 0 V; T_j = 25 °C; see Figure 11	-	0.85	1.5	V
Q_r	recovered charge	V_{GS} = 0 V; I_S = 300 mA; dI_S/dt = -100 A/µs	-	30	-	nC
t_{rr}	reverse recovery time		-	30	-	ns



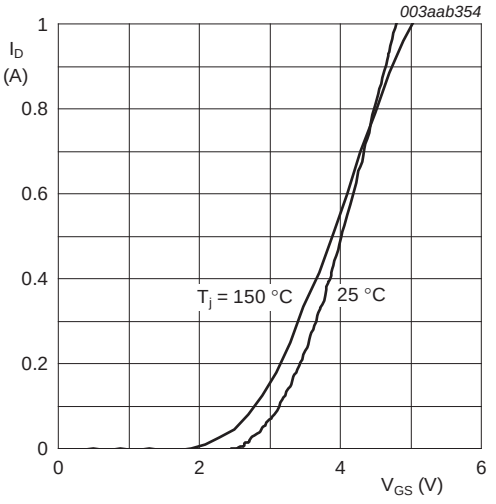
$T_j = 25\,°C$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



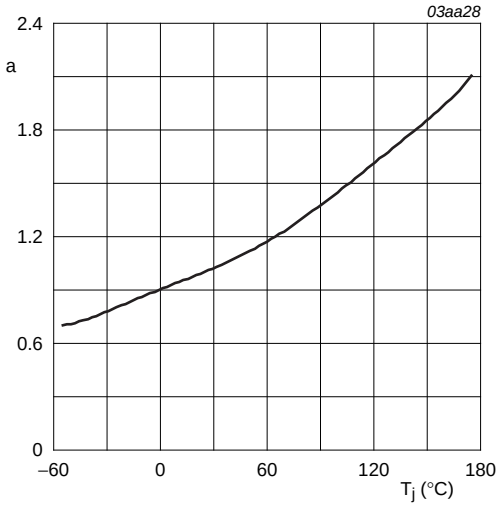
$T_j = 25\,°C$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



$V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature

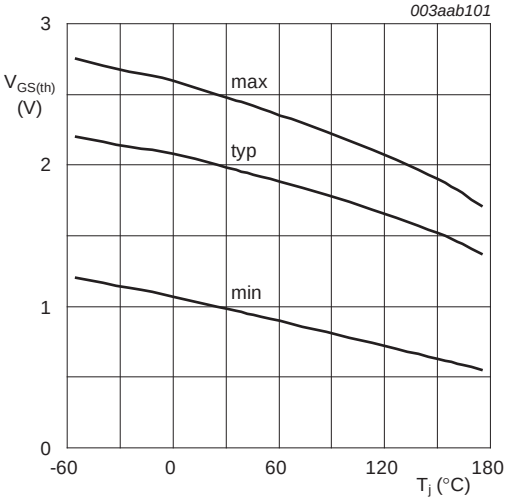


Fig 9. Gate-source threshold voltage as a function of junction temperature

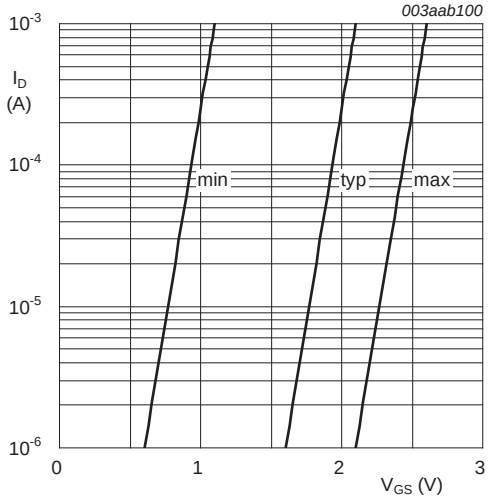
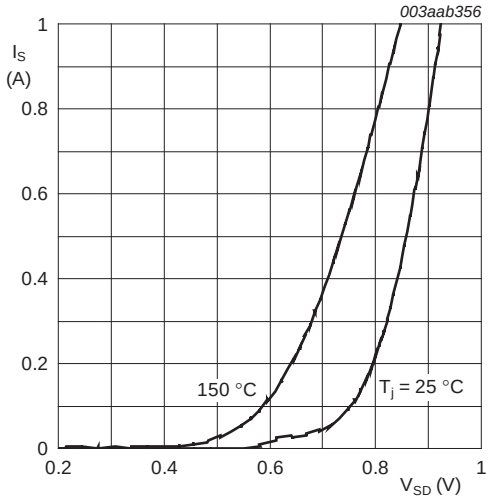
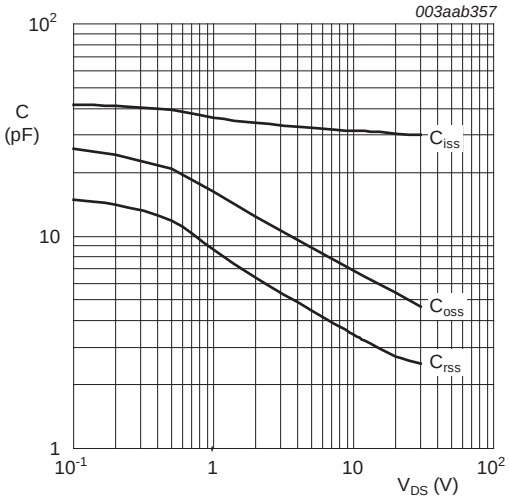


Fig 10. Sub-threshold drain current as a function of gate-source voltage



$V_{GS} = 0\ V$

Fig 11. Source current as a function of source-drain voltage; typical values

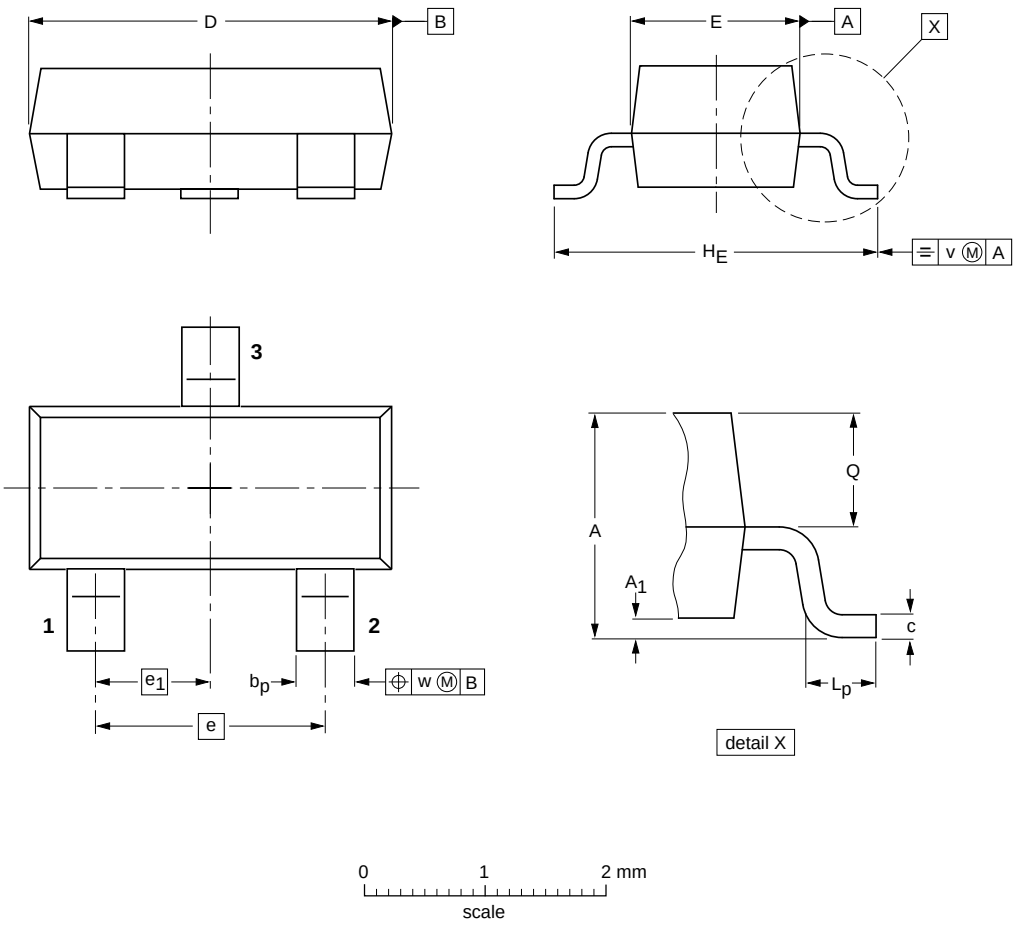


$V_{GS} = 0V; f = 1MHz$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

8. Package outline

Plastic surface-mounted package; 3 leads **SOT23**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT23		TO-236AB				~~04-11-04~~ 06-03-16

Fig 13. Package outline SOT23 (TO-236AB)

9. Soldering

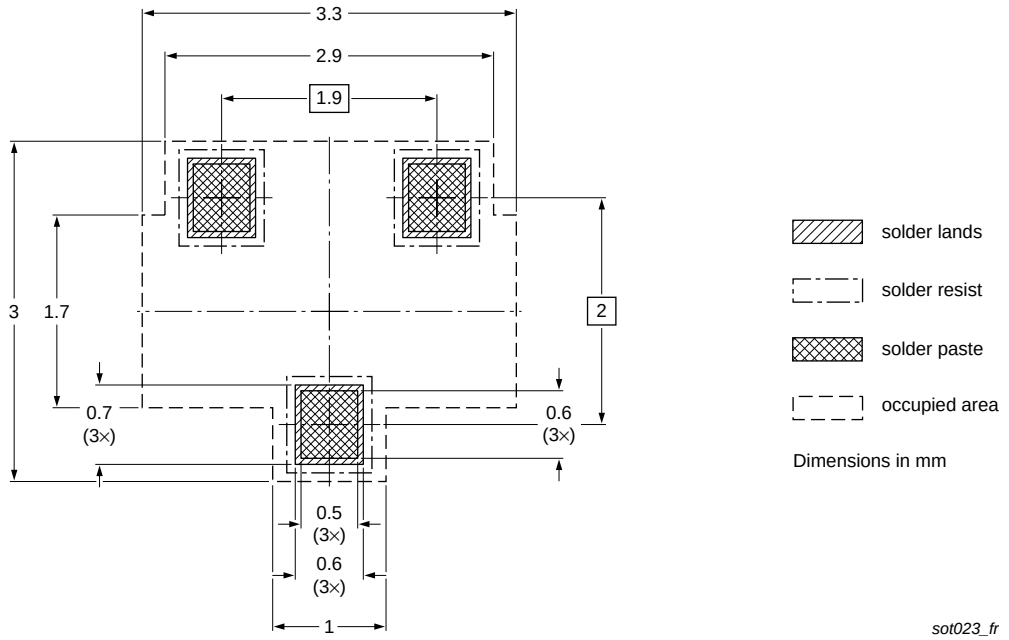


Fig 14. Reflow soldering footprint for SOT23 (TO-236AB)

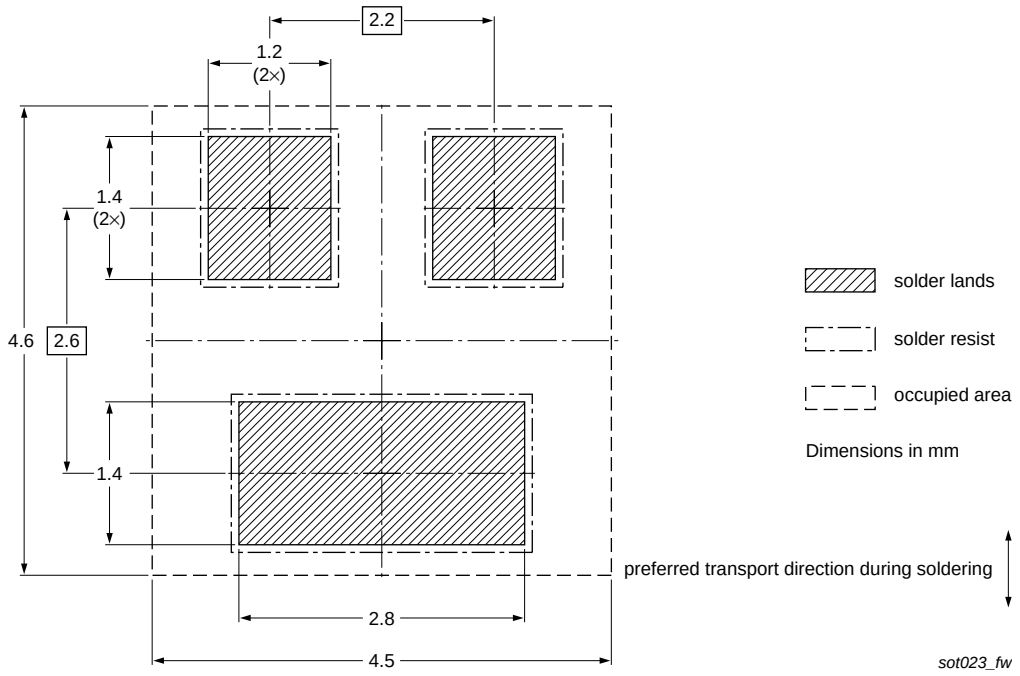


Fig 15. Wave soldering footprint for SOT23 (TO-236AB)

August 2016

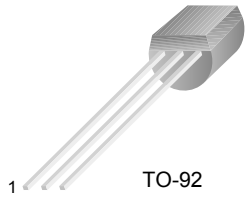
2N7000 / 2N7002 / NDS7002A
N-Channel Enhancement Mode Field Effect Transistor

Features

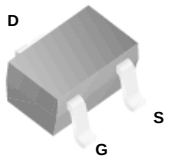
- High Density Cell Design for Low $R_{DS(ON)}$
- Voltage Controlled Small Signal Switch
- Rugged and Reliable
- High Saturation Current Capability

Description

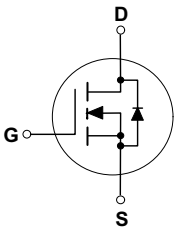
These N-channel enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while providing rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 400 mA DC and can deliver pulsed currents up to 2 A. These products are particularly suited for low-voltage, low-current applications, such as small servo motor control, power MOSFET gate drivers, and other switching applications.



TO-92
1. Source 2. Gate 3. Drain



SOT−23
(TO-236AB)
2N7002/NDS7002A



Ordering Information

Part Number	Marking	Package	Packing Method	Min Order Qty / Immediate Pack Qty
2N7000	2N7000	TO-92 3L	Bulk	10000 / 1000
2N7000_D74Z	2N7000	TO-92 3L	Ammo	2000 / 2000
2N7000_D75Z	2N7000	TO-92 3L	Tape and Reel	2000 / 2000
2N7000_D26Z	2N7000	TO-92 3L	Tape and Reel	2000 / 2000
2N7002	702	SOT-23 3L	Tape and Reel	3000 / 3000
NDS7002A	712	SOT-23 3L	Tape and Reel	3000 / 3000

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_C = 25°C unless otherwise noted.

Symbol	Parameter	Value			Unit
		2N7000	2N7002	NDS7002A	
V_{DSS}	Drain-to-Source Voltage	60			V
V_{DGR}	Drain-Gate Voltage (R_{GS} ≤ 1 MΩ)	60			V
V_{GSS}	Gate-Source Voltage - Continuous	±20			V
	Gate-Source Voltage - Non Repetitive (tp < 50 μS)	±40			
I_D	Maximum Drain Current - Continuous	200	115	280	mA
	Maximum Drain Current - Pulsed	500	800	1500	
P_D	Maximum Power Dissipation Derated above 25°C	400	200	300	mW
		3.2	1.6	2.4	mW/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150		-65 to 150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16-inch from Case for 10 Seconds	300			°C

Thermal Characteristics

Values are at T_C = 25°C unless otherwise noted**.**

Symbol	Parameter	Value			Unit
		2N7000	2N7002	NDS7002A	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	312.5	625	417	°C/W

Electrical Characteristics

Values are at T_C = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Type	Min.	Typ.	Max.	Unit
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 10 μA	All	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V	2N7000			1	μA
		V_{DS} = 48 V, V_{GS} = 0 V, T_C = 125°C				1	mA
		V_{DS} = 60 V, V_{GS} = 0 V	2N7002 NDS7002A			1	μA
		V_{DS} = 60 V, V_{GS} = 0 V, T_C = 125°C				0.5	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 15 V, V_{DS} = 0 V	2N7000			10	nA
		V_{GS} = 20 V, V_{DS} = 0 V	2N7002 NDS7002A			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -15 V, V_{DS} = 0 V	2N7000			-10	nA
		V_{GS} = -20 V, V_{DS} = 0 V	2N7002 NDS7002A			-100	nA

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Type	Min.	Typ.	Max.	Unit
On Characteristics							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA	2N7000	0.8	2.1	3	V
		V_{DS} = V_{GS}, I_D = 250 μA	2N7002 NDS7002A	1	2.1	2.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 500 mA	2N7000		1.2	5	Ω
		V_{GS} = 10 V, I_D = 500 mA, T_C = 125°C			1.9	9	
		V_{GS} = 4.5 V, I_D = 75 mA			1.8	5.3	
		V_{GS} = 10 V, I_D = 500 mA	2N7002		1.2	7.5	
		V_{GS} = 10 V, I_D = 500 mA, T_C = 100°C			1.7	13.5	
		V_{GS} = 5 V, I_D = 50 mA			1.7	7.5	
		V_{GS} = 5 V, I_D = 50 mA, T_C = 100°C			2.4	13.5	
		V_{GS} = 10 V, I_D = 500 mA	NDS7002A		1.2	2	
		V_{GS} = 10 V, I_D = 500 mA, T_C = 125°C			2	3.5	
		V_{GS} = 5 V, I_D = 50 mA			1.7	3	
		V_{GS} = 5 V, I_D = 50 mA, T_C = 125°C			2.8	5	
$V_{DS(ON)}$	Drain-Source On-Voltage	V_{GS} = 10 V, I_D = 500 mA	2N7000		0.6	2.5	V
		V_{GS} = 4.5 V, I_D = 75 mA			0.14	0.4	
		V_{GS} = 10 V, I_D = 500 mA	2N7002		0.6	3.75	
		V_{GS} = 5.0 V, I_D = 50 mA			0.09	1.5	
		V_{GS} = 10 V, I_D = 500 mA	NDS7002A		0.6	1	
		V_{GS} = 5.0 V, I_D = 50 mA			0.09	0.15	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 10 V	2N7000	75	600		mA
		V_{GS} = 10 V, $V_{DS} \geq 2\ V_{DS(on)}$	2N7002	500	2700		
		V_{GS} = 10 V, $V_{DS} \geq 2\ V_{DS(on)}$	NDS7002A	500	2700		
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 200 mA	2N7000	100	320		mS
		$V_{DS} \geq 2V_{DS(ON)}$, I_D = 200 mA	2N7002	80	320		
		$V_{DS} \geq 2V_{DS(ON)}$, I_D = 200 mA	NDS7002A	80	320		

Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Type	Min.	Typ.	Max.	Unit
Dynamic Characteristics							
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	All		20	50	pF
C_{oss}	Output Capacitance		All		11	25	
C_{rss}	Reverse Transfer Capacitance		All		4	5	
t_{on}	Turn-On Time	V_{DD} = 15 V, R_L = 25 Ω, I_D = 500 mA, V_{GS}= 10 V, R_{GEN} = 25 Ω	2N7000			10	ns
		V_{DD} = 30 V, R_L = 150 Ω, I_D = 200 mA, V_{GS}= 10 V, R_{GEN} = 25 Ω	2N7002 NDS7002A			20	
t_{off}	Turn-Off Time	V_{DD} = 15 V, R_L = 25 Ω , I_D = 500 mA, V_{GS}= 10 V, R_{GEN} = 25 Ω	2N7000			10	ns
		V_{DD} = 30 V, R_L = 150 Ω, I_D = 200 mA, V_{GS}= 10 V, R_{GEN} = 25 Ω	2N7002 NDS7002A			20	
Drain-Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		2N7002			115	mA
			NDS7002A			280	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		2N7002			0.8	A
			NDS7002A			1.5	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 115 mA(1)	2N7002		0.88	1.5	V
		V_{GS} = 0 V, I_S = 400 mA(1)	NDS7002A		0.88	1.2	

Note:

1. Pulse test : Pulse Width ≤ 300 μs, Duty Cycel ≤ 2 %.

Typical Performance Characteristics

2N7000 / 2N7002 / NDS7002A

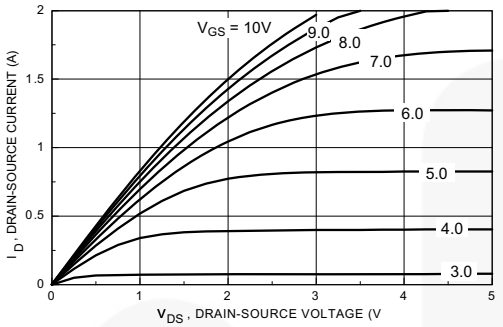


Figure 1. On-Region Characteristics

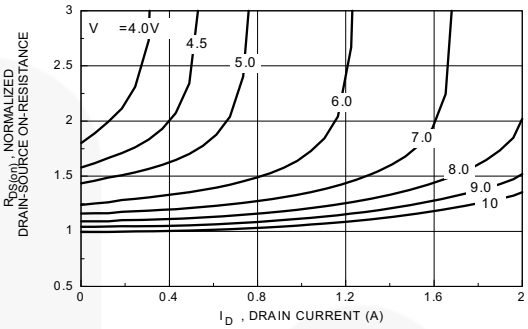


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

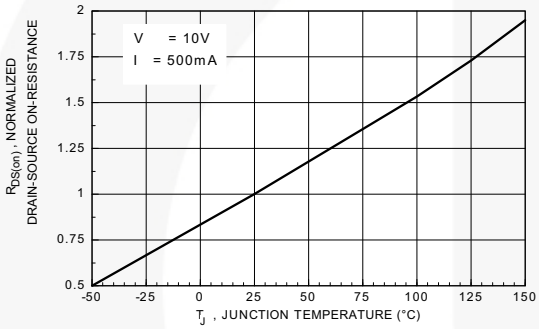


Figure 3. On-Resistance Variation with Temperature

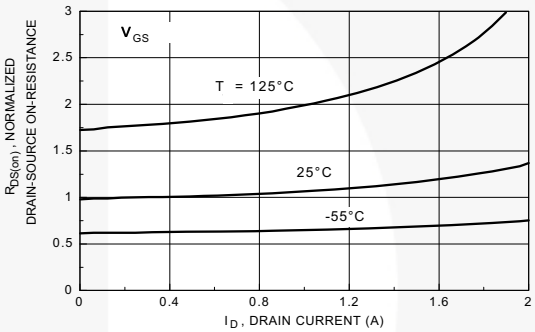


Figure 4. On-Resistance Variation with Drain Current and Temperature

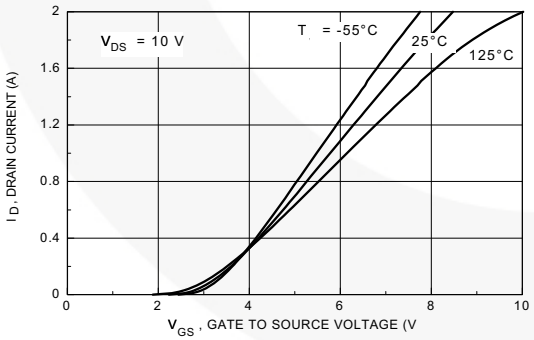


Figure 5. Transfer Characteristics

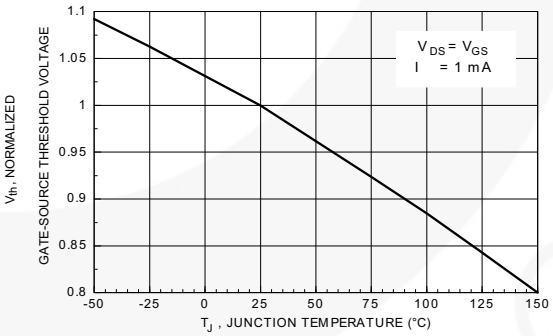


Figure 6. Gate Threshold Variation with Temperature

Typical Performance Characteristics (Continued)

2N7000 / 2N7002 / NDS7002A

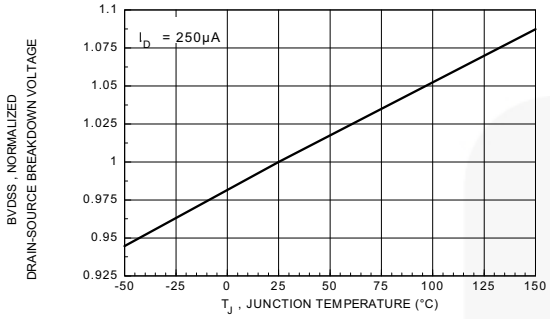


Figure 7. Breakdown Voltage Variation with Temperature

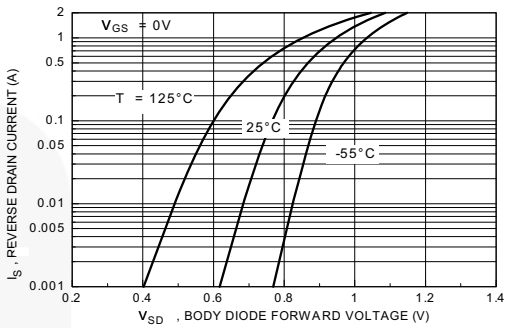


Figure 8. Body Diode Forward Voltage Variation with

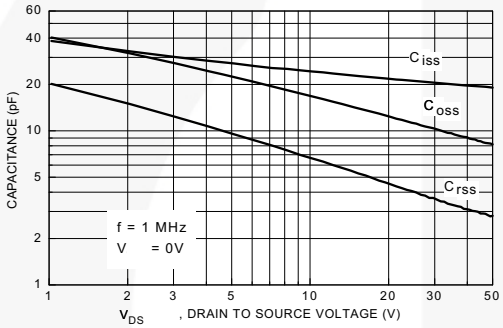


Figure 9. Capacitance Characteristics

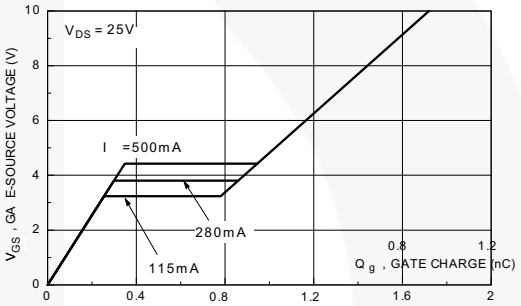


Figure 10. Gate Charge Characteristics

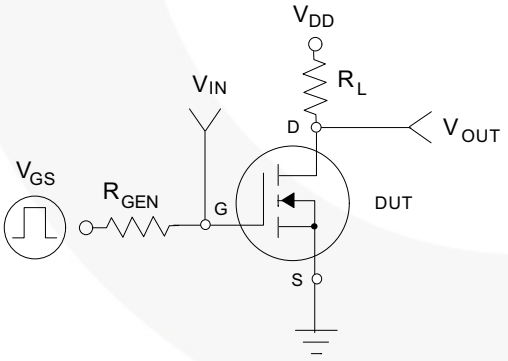


Figure 11. Switching Test Circuit

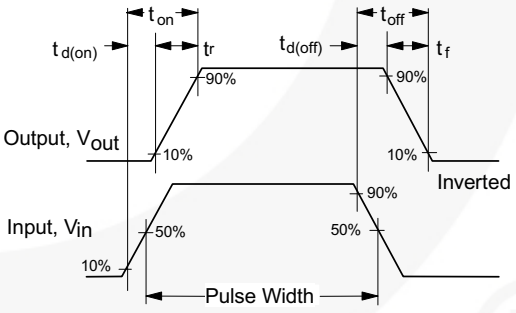


Figure 12. Switching Waveforms

Typical Performance Characteristics (Continued)

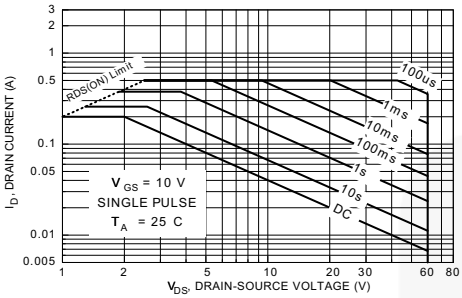


Figure 13. 2N7000 Maximum Safe Operating Area

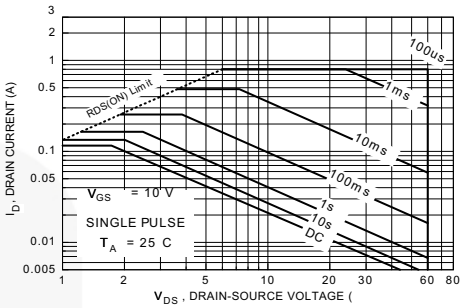


Figure 14. 2N7002 Maximum Safe Operating Area

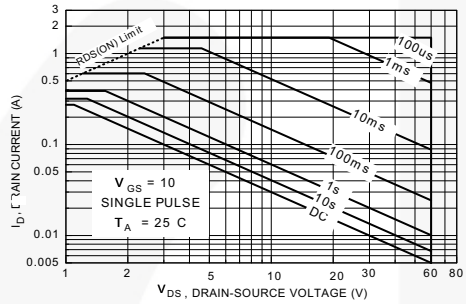


Figure 15. NDS7000A Maximum Safe Operating Area

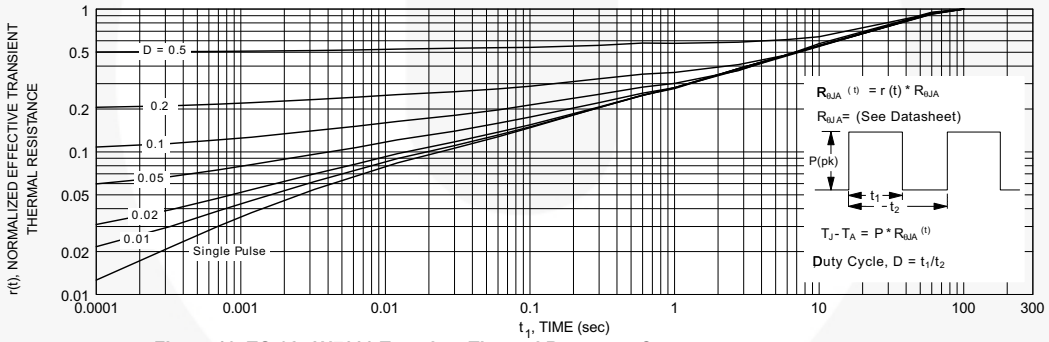


Figure 16. TO-92, 2N7000 Transient Thermal Response Curve

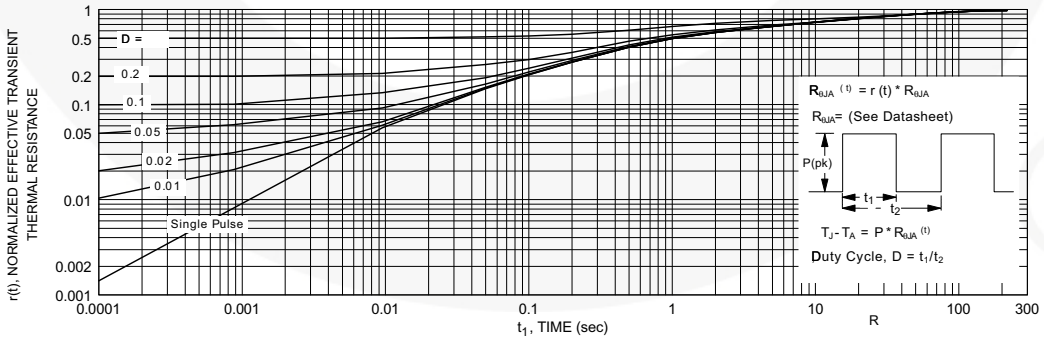
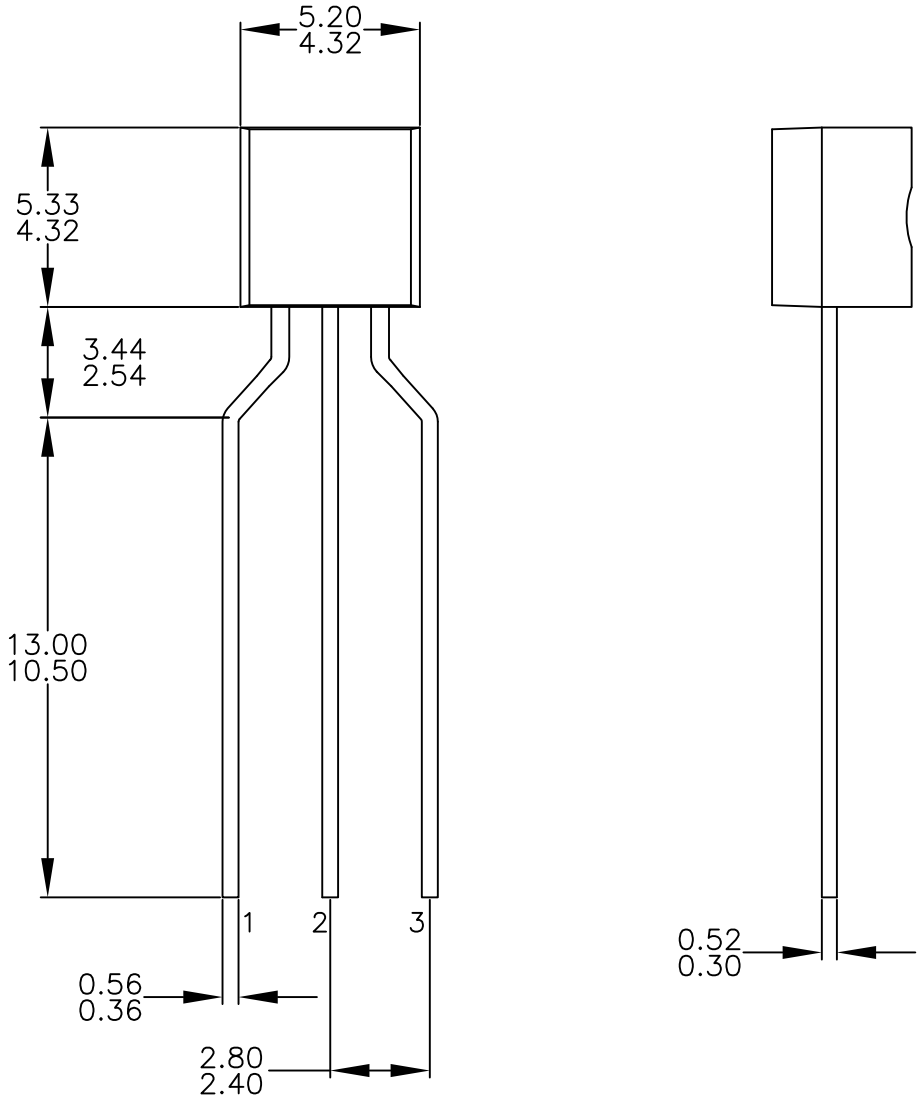
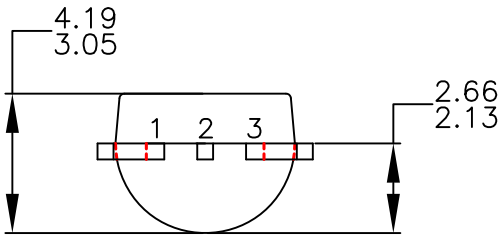


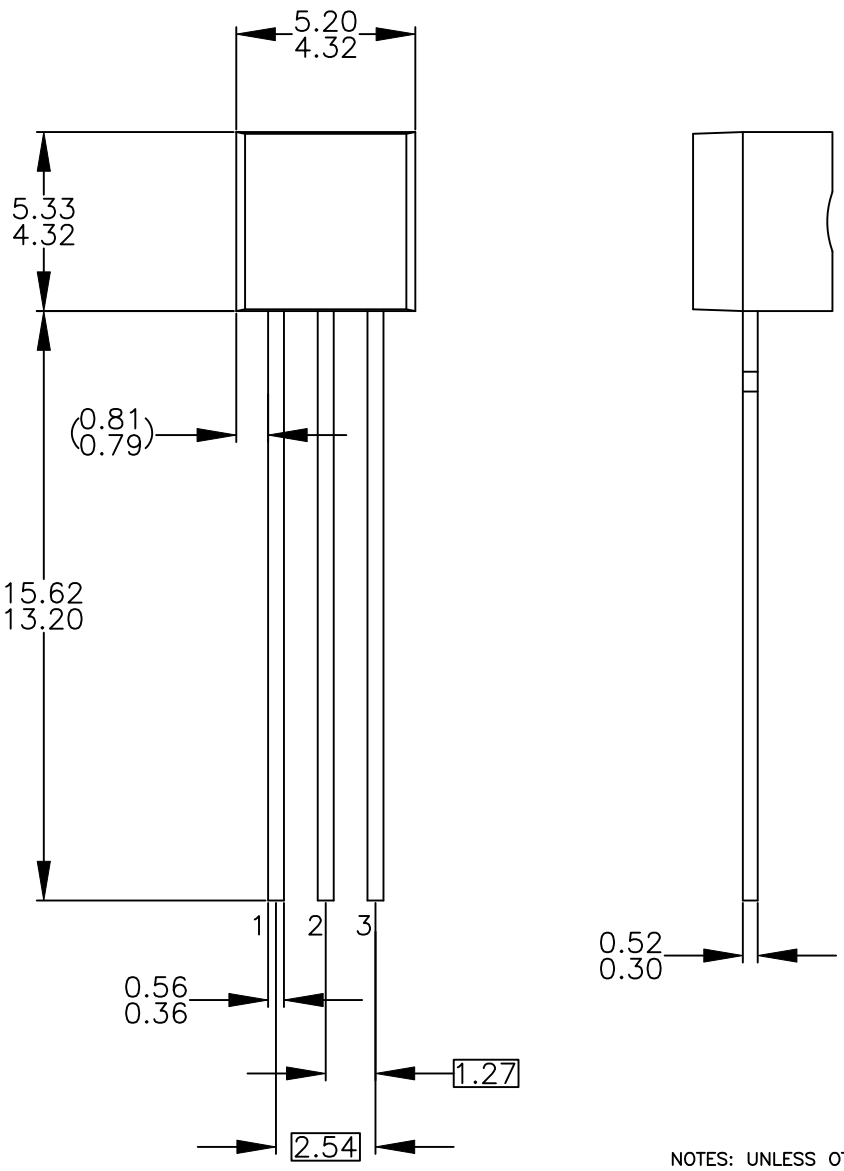
Figure 17. SOT-23, 2N7002 / NDS7002A Transient Thermal Response Curve

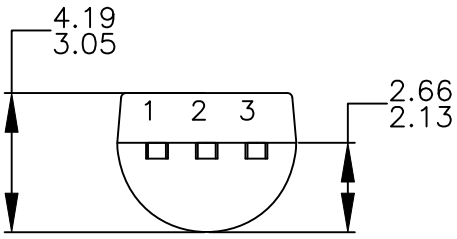




NOTES: UNLESS OTHERWISE SPECIFIED

A. DRAWING CONFORMS TO JEDEC MS-013, VARIATION AC.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5M-2009.
D. DRAWING FILENAME: MKT-ZA03FREV3.
E. FAIRCHILD SEMICONDUCTOR.

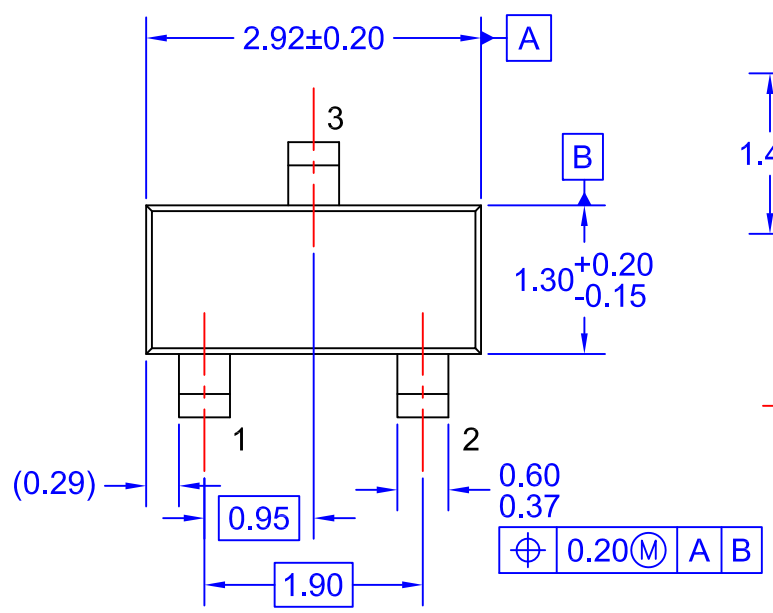


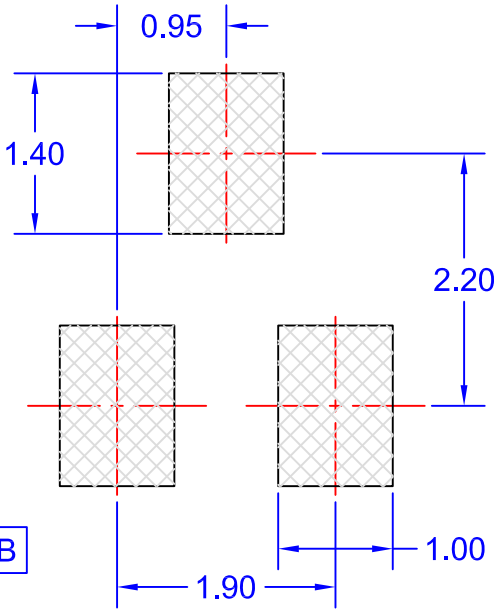


NOTES: UNLESS OTHERWISE SPECIFIED

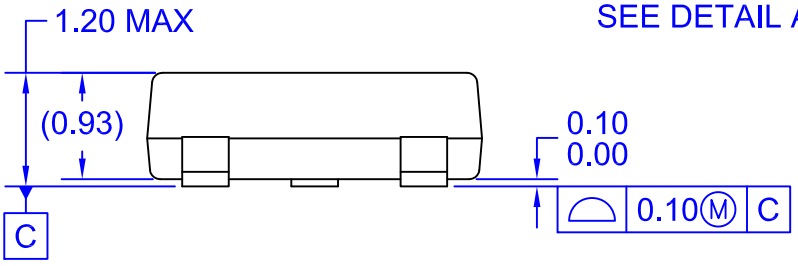
A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M-2009.
D) DRAWING FILENAME: MKT-ZA03DREV4.

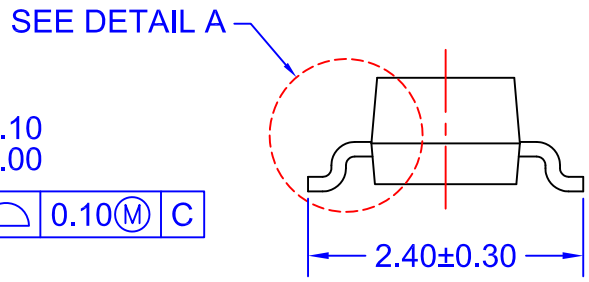
FAIRCHILD

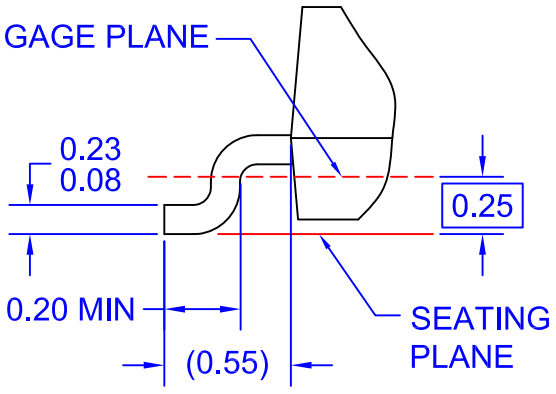




LAND PATTERN
RECOMMENDATION







DETAIL A
SCALE: 2X

NOTES: UNLESS OTHERWISE SPECIFIED

A) REFERENCE JEDEC REGISTRATION TO-236, VARIATION AB, ISSUE H.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 2009.
E) DRAWING FILE NAME: MA03DREV12

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