74HC164; 74HCT164

8-bit serial-in, parallel-out shift register

Rev. 8 — 19 November 2015 Product data sheet

1. General description

The 74HC164; 74HCT164 is an 8-bit serial-in/parallel-out shift register. The device features two serial data inputs (DSA and DSB), eight parallel data outputs (Q0 to Q7). Data is entered serially through DSA or DSB and either input can be used as an active HIGH enable for data entry through the other input. Data is shifted on the LOW-to-HIGH transitions of the clock (CP) input. A LOW on the master reset input (MR) clears the register and forces all outputs LOW, independently of other inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Input levels:
  - For 74HC164: CMOS level
  - For 74HCT164: TTL level
- Gated serial data inputs
- Asynchronous master reset
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from −40 °C to +85 °C and −40 °C to +125 °C.

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC164D	−40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT164D				
74HC164DB	−40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HCT164DB				
74HC164PW	−40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT164PW				
74HC164BQ	−40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74HCT164BQ				

4. Functional diagram

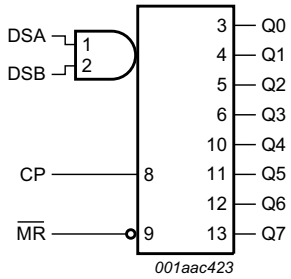


Fig 1. Logic symbol

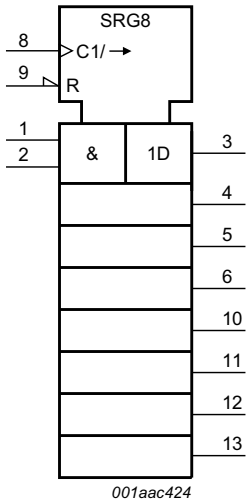


Fig 2. IEC logic symbol

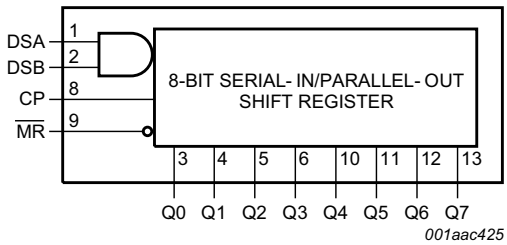


Fig 3. Logic diagram

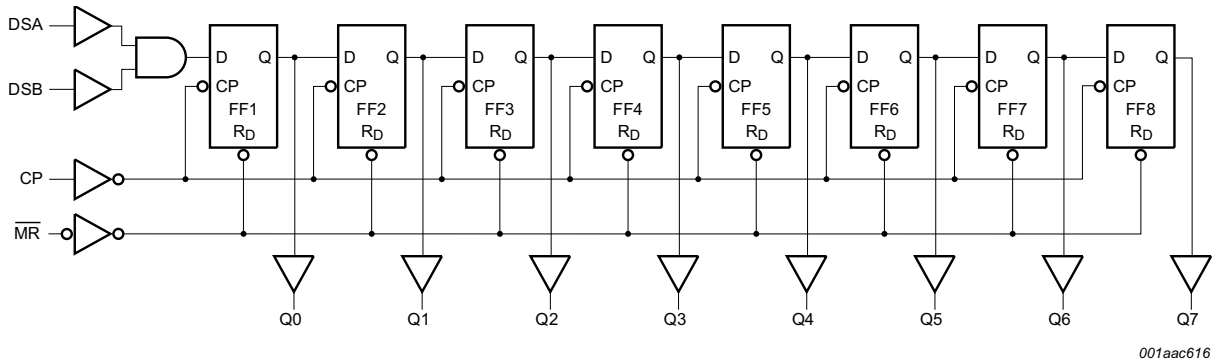


Fig 4. Functional diagram

5. Pinning information

5.1 Pinning

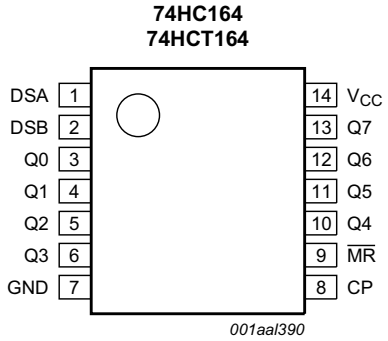
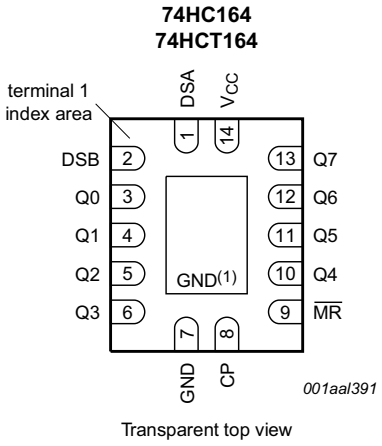


Fig 5. Pin configuration SO14, (T)SSOP14



Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 6. Pin configuration DHVQFN14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
DSA	1	data input
DSB	2	data input
Q0 to Q7	3, 4, 5, 6, 10, 11, 12, 13	output
GND	7	ground (0 V)
CP	8	clock input (LOW-to-HIGH, edge-triggered)
$\overline{MR}$	9	master reset input (active LOW)
V_{CC}	14	positive supply voltage

6. Functional description

Table 3. Function table[1]

Operating modes	Input				Output	
	$\overline{MR}$	CP	DSA	DSB	Q0	Q1 to Q7
Reset (clear)	L	X	X	X	L	L to L
Shift	H	↑	l	l	L	q0 to q6
	H	↑	l	h	L	q0 to q6
	H	↑	h	l	L	q0 to q6
	H	↑	h	h	H	q0 to q6

[1] H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
q = lower case letters indicate the state of the referenced input one set-up time prior to the LOW-to-HIGH clock transition
↑ = LOW-to-HIGH clock transition

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			−50	-	mA
T_{stg}	storage temperature			−65	+150	°C

Table 4. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{tot}	total power dissipation	SO14, (T)SSOP14 and DHVQFN14 packages	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For (T)SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC164			74HCT164			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC164										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = –4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V

Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT164										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = –20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8	-	80	-	160	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC}$ – 2.1 V; I_O = 0 A; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V	-	100	360	-	450	-	490	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; test circuit see Figure 10; unless otherwise specified

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC164										
t_{pd}	propagation delay	CP to Qn; see Figure 7 [1]								
		V_{CC} = 2.0 V	-	41	170	-	215	-	255	ns
		V_{CC} = 4.5 V	-	15	34	-	43	-	51	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	12	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	12	29	-	37	-	43	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; see Figure 8								
		V_{CC} = 2.0 V	-	39	140	-	175	-	210	ns
		V_{CC} = 4.5 V	-	14	28	-	35	-	42	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	11	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	11	24	-	30	-	36	ns
t_t	transition time	see Figure 7 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_W	pulse width	CP HIGH or LOW; see Figure 7								
		V_{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	4	-	17	-	20	-	ns
		MR LOW; see Figure 8								
		V_{CC} = 2.0 V	60	17	-	75	-	90	-	ns
		V_{CC} = 4.5 V	12	6	-	15	-	18	-	ns
		V_{CC} = 6.0 V	10	5	-	13	-	15	-	ns
t_{rec}	recovery time	$\overline{MR}$ to CP; see Figure 8								
		V_{CC} = 2.0 V	60	17	-	75	-	90	-	ns
		V_{CC} = 4.5 V	12	6	-	15	-	18	-	ns
		V_{CC} = 6.0 V	10	5	-	13	-	15	-	ns
t_{su}	set-up time	DSA, and DSB to CP; see Figure 9								
		V_{CC} = 2.0 V	60	8	-	75	-	90	-	ns
		V_{CC} = 4.5 V	12	3	-	15	-	18	-	ns
		V_{CC} = 6.0 V	10	2	-	13	-	15	-	ns
t_h	hold time	DSA, and DSB to CP; see Figure 9								
		V_{CC} = 2.0 V	+4	–6	-	4	-	4	-	ns
		V_{CC} = 4.5 V	+4	–2	-	4	-	4	-	ns
		V_{CC} = 6.0 V	+4	–2	-	4	-	4	-	ns

Table 7. Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; test circuit see Figure 10; unless otherwise specified

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
f_{max}	maximum frequency	for Cp, see Figure 7								
		V_{CC} = 2.0 V	6	23	-	5	-	4	-	MHz
		V_{CC} = 4.5 V	30	71	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	78	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	35	85	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC} [3]	-	40	-	-	-	-	-	pF
74HCT164										
t_{pd}	propagation delay	CP to Qn; see Figure 7 [1]								
		V_{CC} = 4.5 V	-	17	36	-	45	-	54	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	14	-	-	-	-	-	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; see Figure 8								
		V_{CC} = 4.5 V	-	19	38	-	48	-	57	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	16	-	-	-	-	-	ns
t_t	transition time	see Figure 7 [2]								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t_W	pulse width	CP HIGH or LOW; see Figure 7								
		V_{CC} = 4.5 V	18	7	-	23	-	27	-	ns
		MR LOW; see Figure 8								
		V_{CC} = 4.5 V	18	10	-	23	-	27	-	ns
t_{rec}	recovery time	$\overline{MR}$ to CP; see Figure 8								
		V_{CC} = 4.5 V	16	7	-	20	-	24	-	ns
t_{su}	set-up time	DSA, and DSB to CP; see Figure 9								
		V_{CC} = 4.5 V	12	6	-	15	-	18	-	ns
t_h	hold time	DSA, and DSB to CP; see Figure 9								
		V_{CC} = 4.5 V	+4	–2	-	4	-	4	-	ns
f_{max}	maximum frequency	for Cp, see Figure 7								
		V_{CC} = 4.5 V	27	55	-	22	-	18	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	61	-	-	-	-	-	MHz

Table 7. Dynamic characteristics *...continued*

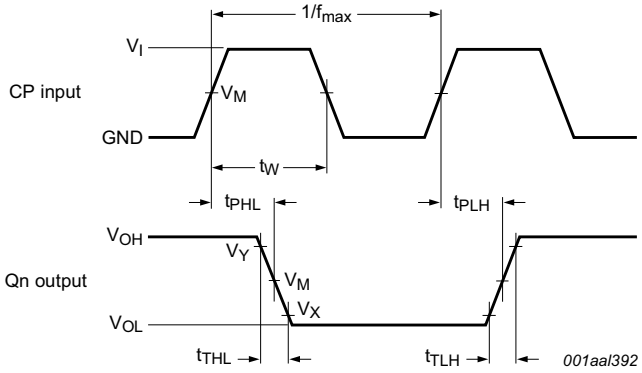
GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; test circuit see Figure 10; unless otherwise specified

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_{PD}	power dissipation capacitance	per package; [3] V_I = GND to V_{CC} – 1.5 V	-	40	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.



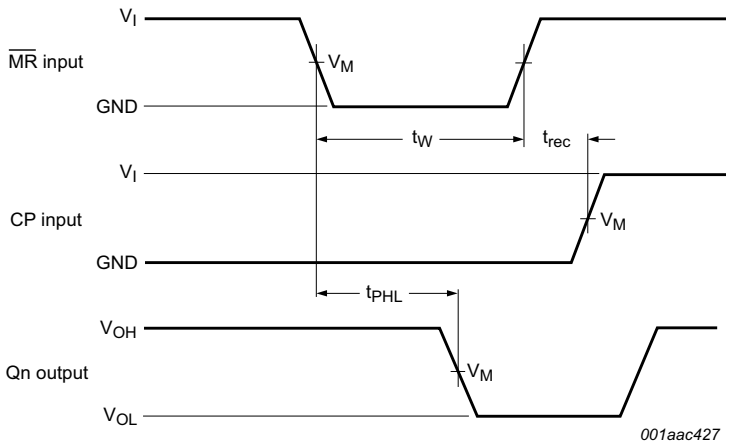
(1) Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Waveforms showing the clock (CP) to output (Qn) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency

Table 8. Measurement points

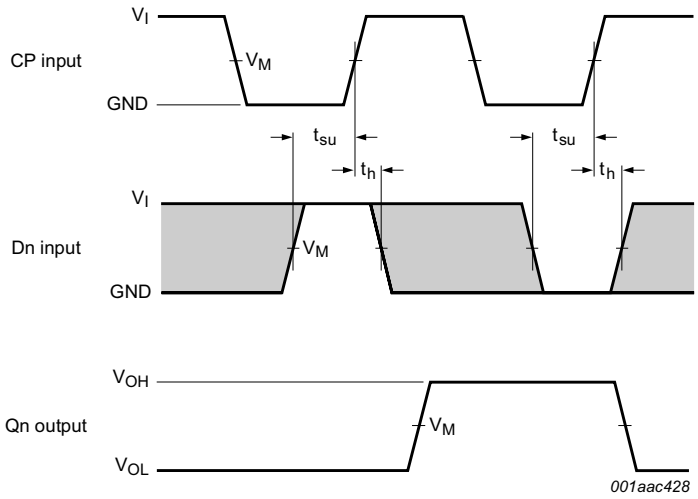
Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC164	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT164	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$



(1) Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. Waveforms showing the master reset ($\overline{MR}$) pulse width, the master reset to output (Qn) propagation delays and the master reset to clock (CP) removal time

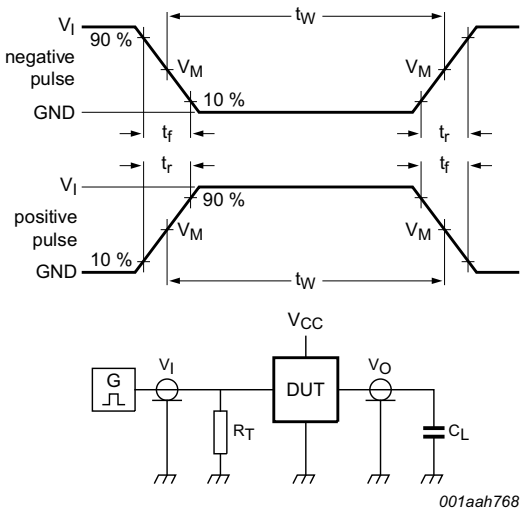


(1) Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 9. Waveforms showing the data set-up and hold times for Dn inputs



Test data is given in Table 9.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

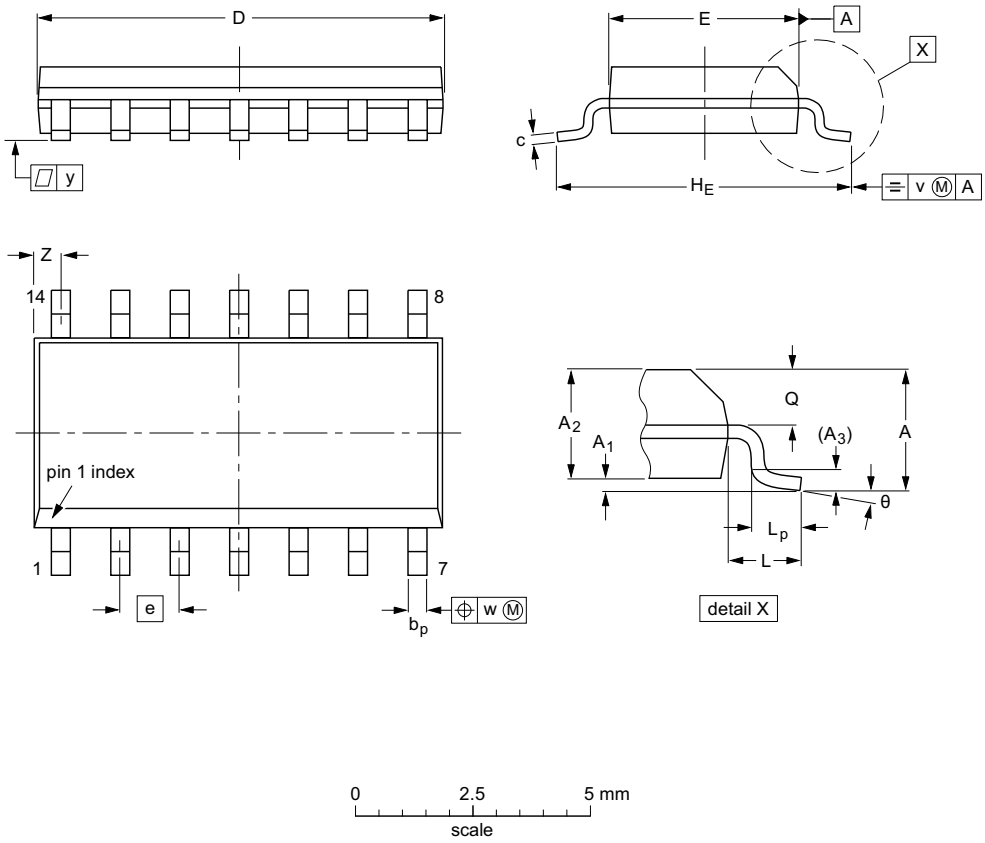
Fig 10. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC164	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT164	3.0 V	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

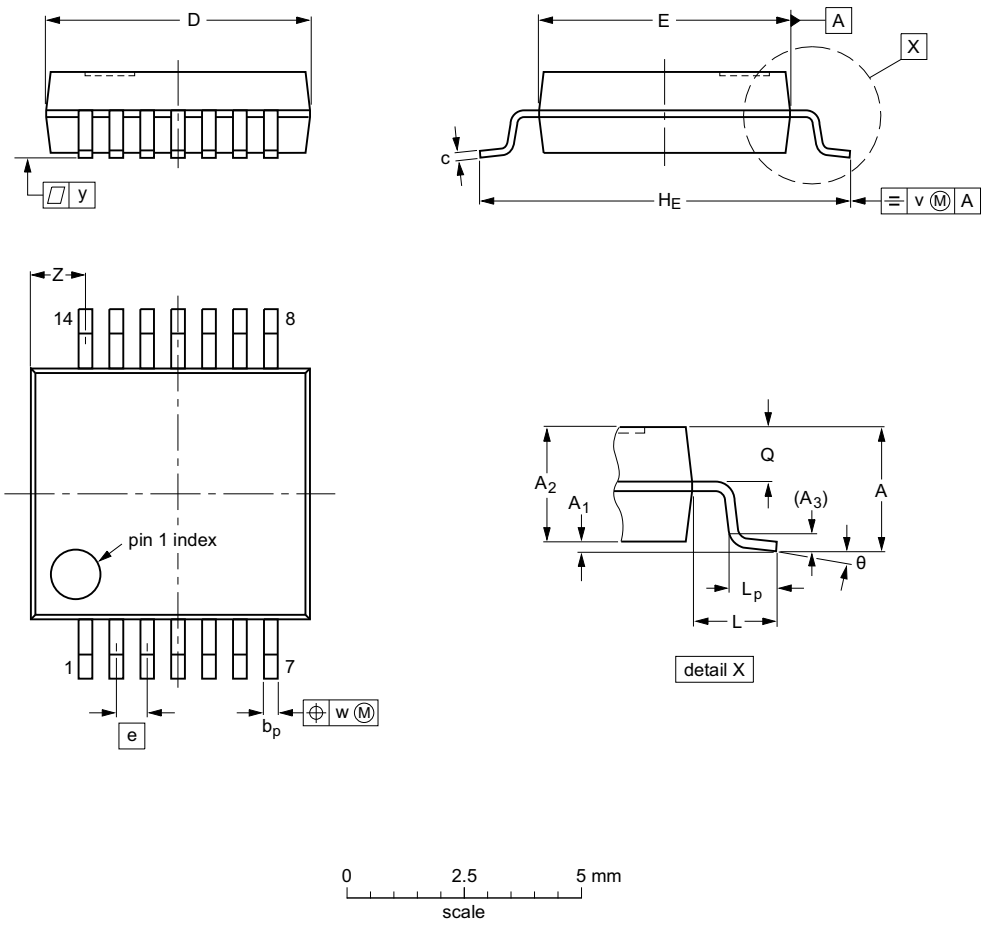
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

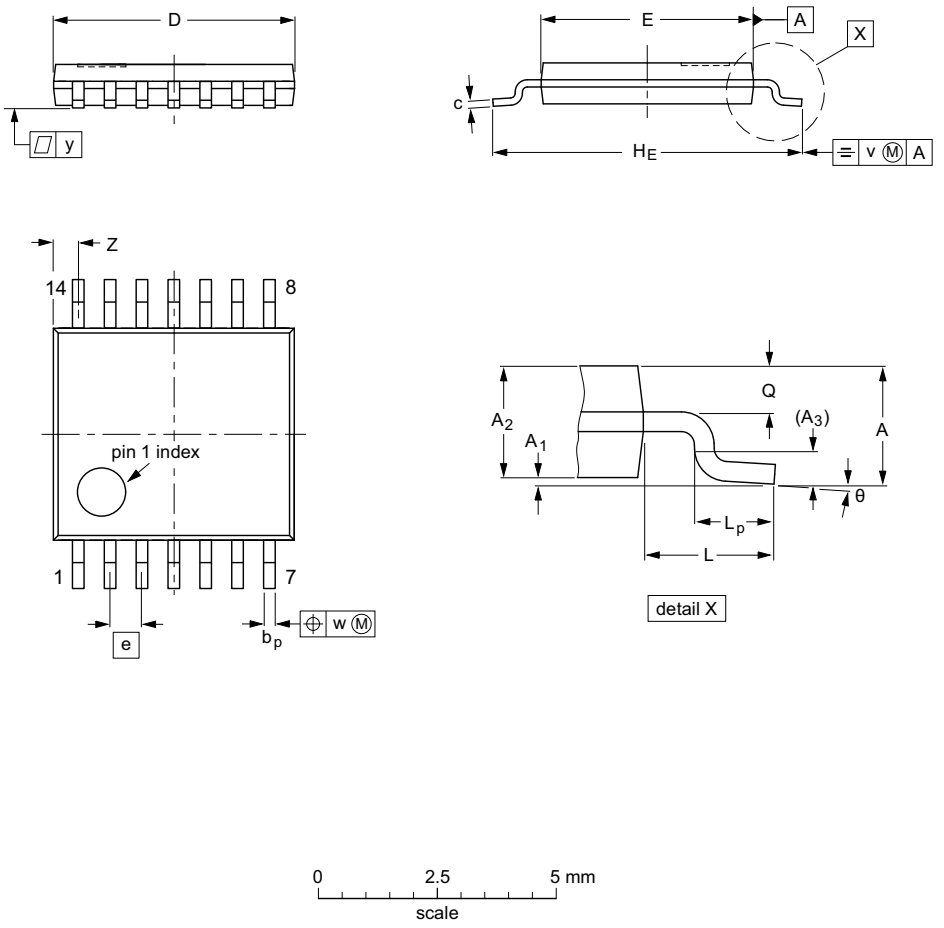
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

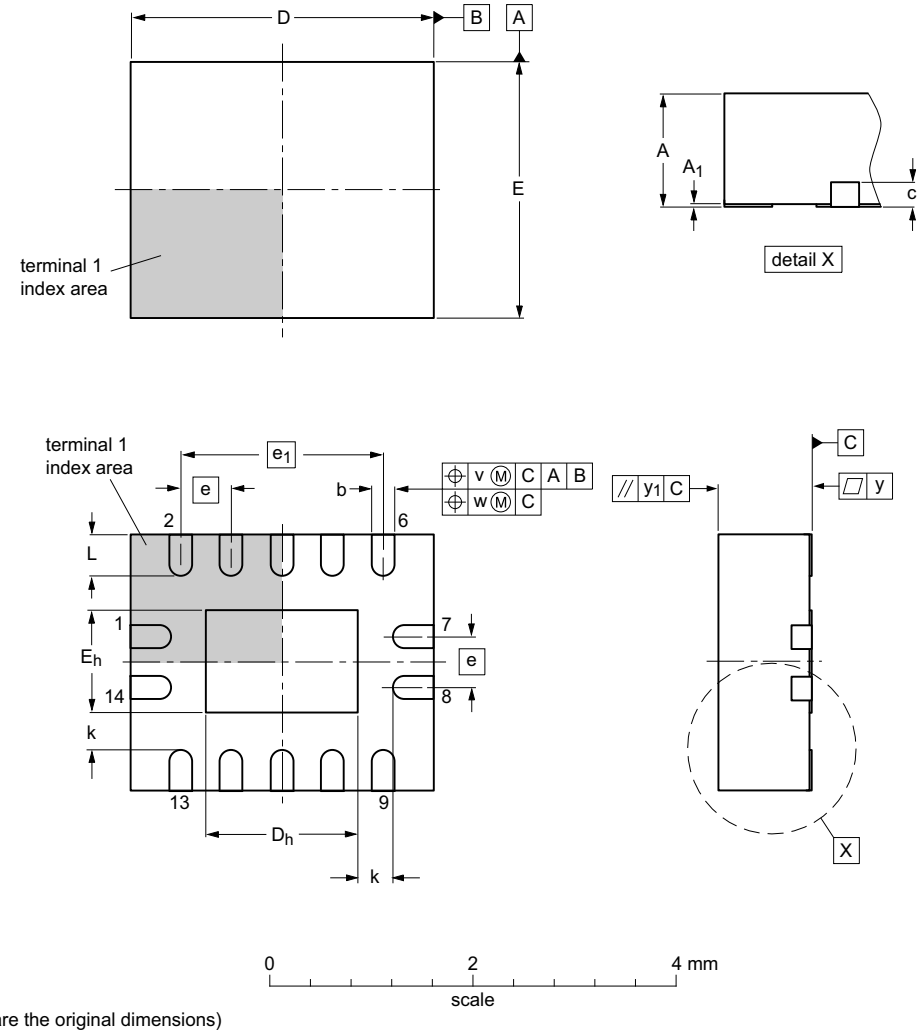
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 13. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	k	L	v	w	y	y_1
	max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
mm	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				~~15-04-10~~ 15-05-05

Fig 14. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT164 v.8	20151119	Product data sheet	-	74HC_HCT164 v.7
Modifications:	• Type numbers 74HC164N and 74HCT164N (SOT27-1) removed.			
74HC_HCT164 v.7	20130613	Product data sheet	-	74HC_HCT164 v.6
Modifications:	• General description updated.			
74HC_HCT164 v.6	20111212	Product data sheet	-	74HC_HCT164 v.5
Modifications:	• Legal pages updated.			
74HC_HCT164 v.5	20101125	Product data sheet	-	74HC_HCT164 v.4
74HC_HCT164 v.4	20100202	Product data sheet	-	74HC_HCT164 v.3
74HC_HCT164 v.3	20050404	Product data sheet	-	74HC_HCT164_ CNV v.2
74HC_HCT164_CNV v.2	19901201	Product specification	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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